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The Alpha 21264 Microprocessor Architecture RE Kessler, EJ McLellan, and DA Webb ... -

► [virginia.edu](#) [PDF]

RE Kessler - ... International Conference on Computer Design: VLSI ..., 1998 - doi.ieeecomputersociety.org

... It would be incorrect if a later **load** issued prior to ... not return the value of the earlier **store** to the ... not know the memory **address** before the **instruction** issues ...

Cited by 671 - Related articles - BL Direct - All 96 versions

Speculative execution via address prediction and data prefetching- ► [psu.edu](#) [PDF]

J González, A González - Proceedings of the 11th international conference on ..., 1997 - portal.acm.org

... gathered in previous executions of that static **load/store**. Predicted loads and stores are issued speculatively ... Instructions that depend on speculative loads are ...

Cited by 120 - Related articles - All 16 versions

Value locality and load value prediction- ► [isu.edu](#) [PDF]

MH Lipasti, CB Wilkerson, JP Shen - ACM SIGOPS Operating Systems Review, 1996 - portal.acm.org

... **load** value prediction, unlike other speculative tech- niques ... in Figure 3 for both loads and stores. ... the low-order bits of the **load instruction address** are used ...

Cited by 612 - Related articles - BL Direct - All 29 versions

Exceeding the dataflow limit via value prediction- ► [psu.edu](#) [PDF]

MH Lipasti, JP Shen - Proceedings of the 29th annual ACM/IEEE ..., 1996 - portal.acm.org

... uses a value cache to **store** and look ... by exploiting the affinity between **load instruction** addresses and ... LVP table is indexed by **instruction address**, and hence ...

Cited by 450 - Related articles - BL Direct - All 27 versions

Speculative versioning cache- ► [kfupm.edu.sa](#) [PDF]

S Gopal, TN Vijaykumar, JE Smith, GS Sohi - Proceedings of the 4th International Symposium on ..., 1998 - doi.ieeecomputersociety.org

... If a **load** is to the same **address** as a ... **store**, it can use data bypassed from the **store** when the ... constraint of this approach is that a **load instruction** cannot be ...

Cited by 222 - Related articles - All 37 versions

The store-load address table and speculative register promotion- ► [kfupm.edu.sa](#) [PDF]

M Postiff, D Greene, T Mudge - Proceedings of the 33rd annual ACM/IEEE ..., 2000 - portal.acm.org

... Likewise, an unmap **instruction** removes an association from the SLAT, sending ... and unmap operations are essentially just special **load** and **store** operations. ...

Cited by 20 - Related articles - BL Direct - All 12 versions

Dynamic speculative precomputation- ► [ucsd.edu](#) [PDF]

JD Collins, DM Tullisen, H Wang, JP Shen - Proceedings of the 34th annual ACM/IEEE ..., 2001 - portal.acm.org

... Its **address** base is included in a p-slice, the **address** accessed by this **load** is also ... When a **store instruction** (again with the stack register as its base) is ...

Cited by 142 - Related articles - BL Direct - All 11 versions

Speculative register promotion using advanced load address table (alat)- ► [psu.edu](#) [PDF]

J Lin, T Chen, WC Hsu, PC Yew - Code Generation and Optimization, 2003. CGO 2003. ..., 2003 - IEEE Explore IEEE.org

... is issued with a special **load instruction**, **ld.a** ... are stored in an entry for this **speculative load**. Every **store** operation automatically compares its **store address** ...
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Enhancing software reliability with **speculative threads**- ► [psu.edu](#) [PDF]

J Oplinger, MS Lam - [portal.acm.org](#)

... are handled by augmenting the functionality of the **load-store** queues. ... and the program counter is set to the **address** specified by the last **TRY instruction**. ...

Cited by 78 - Related articles - Bk Direct - All 29 versions

... to dynamically control the out-of-order execution of **load-store instructions** in a processor

...

JH Hesson, J LeBlanc, SJ Ciavaglia - US Patent 5,615,350, 1997 - Google Patents

... Floating Point **Instruction PO** • **Instruction Fetch PO** **Instruction Fetch PI** ... prior art by permitting **speculative** execution of **load** and **store instructions**. ...

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